Engineering Tripos Part IIA Project, GB3: RISC-V Processor, 2020-21

Leader

Dr P Stanley-Marbell [1]

Timing and Structure

Fridays 9-11am plus afternoons, and Tuesdays 11-1pm

Prerequisites

3B2 (essential). Prior familiarity with Unix command line tools (e.g., basic shell scripts, creating Makefiles, and so on) and with git and GitHub is desirable.

Aims

The aims of the course are to:

- To become familiar with Verilog HDL and with the Lattice iCE40, a state-of-the-art low-power miniature FPGA used in many commercial embedded sensing and wearable computing applications.
- Obtain hands-on experience with implementing ideas relating to a Bayesian view of measurements, measurement uncertainty, sensors, and computing on sensor data on state-of-the-art FPGAs
- To obtain experience working with FPGA synthesis tools for Internet of Things (i.e., embedded sensing and computing) applications.
- To gain experience with the RISC-V (pronounced "RISC-five") architecture, an exciting, new, and forward-looking reduced instruction set computer (RISC) architecture.
- To carry out the implementation and evaluation of a minimal subset of the RISC-V architecture on the iCE40 FPGA.

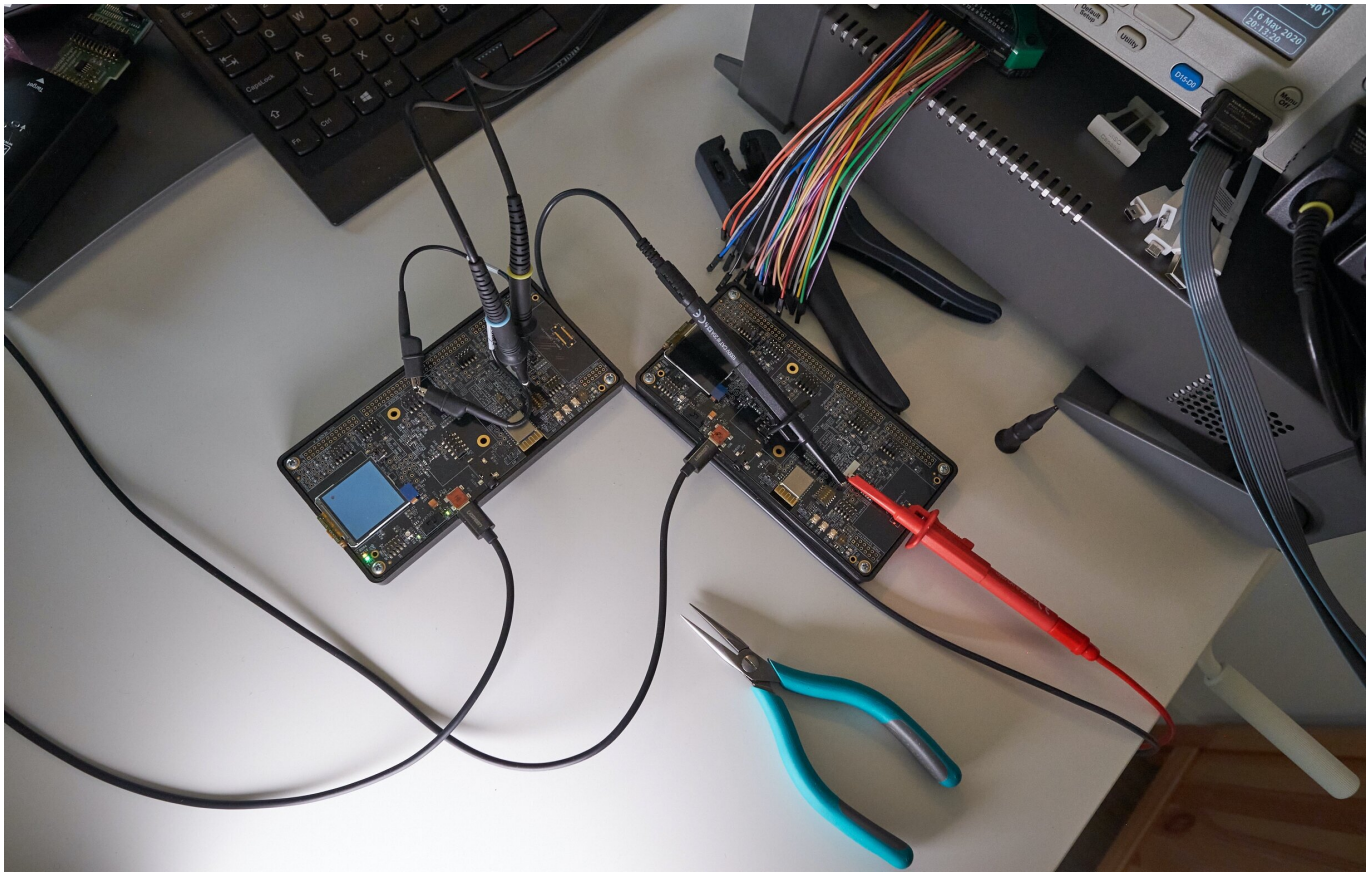
Content

Students will work in groups of three for this project.

Students modify an unoptimized RV32I RISC-V processor running on an iCE40 FPGA in a tiny wafer-scale 2.15x2.50 mm WLCSP package, using a completely open-source toolchain. The hardware used in the project has isolated power rails for the FPGA core, I/O, and PLL. Because the hardware has built-in shunt resistors, students can measure power usage with a laboratory multimeter. Students work in groups of three to evaluate the performance, power dissipation, and resource usage of their modifications and the project culminates in a competition between teams to achieve designs on the Pareto frontier. (One team last year got active power dissipation, while running a provided benchmark, down to 214 microwatts.)

The RISC-V architecture is a new open reduced instruction set computer (RISC) architecture that has many advantages over legacy architectures such as ARM. Because it was designed from the ground up for efficiency, RISC-V enables more efficient hardware implementations than many existing commercial architectures. One variant of the RISC-V is small enough to fit within the Lattice iCE40, a low-power miniature FPGA (in a 2.15x2.55mm package) targeted at embedded sensing / Internet of Things systems. This project will provide students with the opportunity to gain experience with the RISC-V architecture, an exciting, new, and forward-looking reduced instruction set computer (RISC) architecture and to implement and evaluate a minimal subset of the RISC-V architecture on the iCE40 FPGA. Through the project's choice of application examples, this IIA project will also provide hand-on experience with implementing ideas relating to a Bayesian view of measurements, measurement uncertainty, sensors, and computing on sensor data that is synergistic with other research and

teaching in the Department of Engineering at the University of Cambridge.



Week 1

Complete the warm-up exercise mapping the provided pre-implemented RISC-V subset processor core on the iCE40 and become familiar with the open-source FPGA synthesis tools, with the RISC-V processor emulator, and with Verilog. Watch the overview fascicle videos on the toolchain and on a Bayesian view of measurements, measurement uncertainty, sensors, and computing on sensor data.

Week 2

Evaluate design options to improve performance, FPGA resource usage, and power dissipation of the baseline RISC-V processor core.

Week 3

Keeping in mind the goal of Pareto-optimal designs, the three team members implement improvements to the performance, power dissipation, and resource usage of the baseline RISC-V processor.

Week 4

Evaluate the improved design in terms of performance, power dissipation, and FPGA resource usage for the measurement data uncertainty propagation and particle filter benchmark applications.

Coursework

Coursework	Due date	Marks
Interim report 1 (individual credit)	4pm Friday 21st May 2021	20

Report on your characterization of the performance, power dissipation, and FPGA resource usage of the provided baseline RISC-V processor implementation.	(week two)	
Interim report 2 (individual credit) Describe progress improving the implementation of the provided RISC-V processor core in terms of performance, FPGA resource usage, and power dissipation when running on the iCE40 FPGA.	4pm Friday 28th May 2021 (week three)	30
Final report (10 points for group credit for demo, individual credit for report) Demonstration and report on modified RISC-V processor core implementation.	4pm Thursday 10th June 2021 (week five)	30

Examination Guidelines

Please refer to Form & conduct of the examinations [2].

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Links
[1] mailto:ps751@cam.ac.uk
[2] https://teaching26-27.eng.cam.ac.uk/content/form-conduct-examinations