Version OBA/2

EGT2
ENGINEERING TRIPOS PART IIA

Friday 1 May 2026 9.30 to 11.10

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Consider the Verilog code in Fig. 1.

(i) Derive the Boolean expression for the value of `q_out[k]` following a rising clock edge in terms of the inputs `ctrl[k]`, `data_in[k]`, and the current value of `q_out[k]`. [10%]

(ii) Rewrite the `else` branch (lines 13–18) using a single line of behavioural Verilog statement that utilises bitwise operators instead of the `for` loop and `if` statement. [10%]

```
1   module multi_reg (
2       input            clk, rst,
3       input [3:0]      data_in,
4       input [3:0]      ctrl,
5       output reg [3:0] q_out
6   );
7   integer k;
8
9   always @(posedge clk or posedge rst) begin
10      if (rst)
11          q_out <= 4'b0000;
12      else begin
13          for (k = 0; k < 4; k = k + 1) begin
14              if (ctrl[k])
15                  q_out[k] <= ~q_out[k];
16              else
17                  q_out[k] <= data_in[k];
18          end
19      end
20  end
21  endmodule
```

Fig. 1

(cont.

(b) Design a sequential circuit using T bistables that continuously cycles through a sequence of states representing a subset of Fibonacci numbers: {1, 2, 3, 5, 8, 13}. Each state is represented by its 4-bit binary numbers, e.g., 1=0001, 13=1101. The counter transitions to the next state in the sequence on each clock pulse, returning to 1 after reaching 13. The circuit has a single output, Z. $Z = 1$ when the current state is 1, 5, or 8. $Z = 0$ when the current state is 2, 3, or 13. Assume all unused states as "don't care" conditions.

(i) Draw the state diagram for this circuit. [5%]

(ii) Build the state table for this circuit. [20%]

(iii) Derive the minimised input functions for the bistables and minimised output function for the circuit. [20%]

(iv) Draw the circuit implementation for this counter using T bistables and logic gates. [20%]

(c) Briefly discuss the advantages and disadvantages of implementing logic functions with ROMs, LUTs, and PLAs. [15%]

2 (a) Consider the circuit in Fig. 2.

(i) Build the state table for this circuit. [10%]

(ii) Is the circuit a Mealy or Moore circuit? Justify your answer. [10%]

(iii) Does the circuit have any unused states? Assume 00 is the initial state. [10%]

(iv) What is the output sequence for the input sequence $X = 01100$ when it is applied in the order of 0 (first), 1, 1, 0, 0 (last)? [10%]

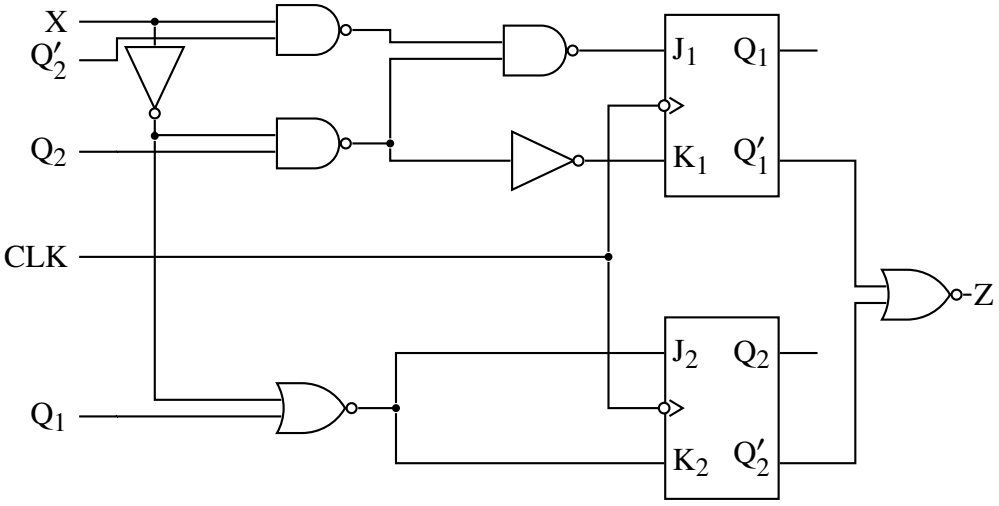

Fig. 2

(cont.

(b) A 4-input LUT is often used as the basic building block of an FPGA.

(i) Show how a 4-input LUT can be implemented by combining two 3-input LUTs and a 2-to-1 multiplexer. [15%]

(ii) Consider the implementation of a comparator circuit in Fig. 3. Determine the logic expressions for F_{01} and F_{23} so that the circuit sets $S_{A=B}$ to 1 when the two binary numbers, $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$, are equal. [15%]

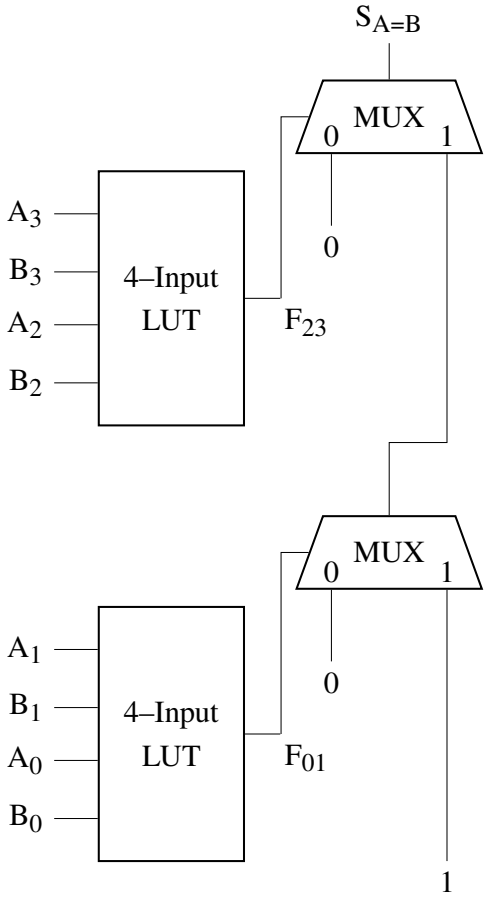

Fig. 3

(c) Design a Mealy-type synchronous sequential controller circuit for a vending machine that dispenses two different meals: A (for £ 1.50) and B (for £ 2.50). The machine has a selection switch that captures the user's choice, and has a single coin slot that accepts 50 p, £ 1, and £ 2, one coin at a time. If the accumulated credit equals or exceeds the price of the selected meal, the machine dispenses corresponding meal and resets. Assume that the machine does not give any change. Clearly state any other assumption that you make in your design.

(i) Build the state table for this circuit. [15%]

(ii) Draw the circuit implementation for this controller using ROM. [15%]

3 (a) The voltage transfer characteristic of an inverter is shown in Fig. 4. The supply voltage V_{DD} is 5 V.

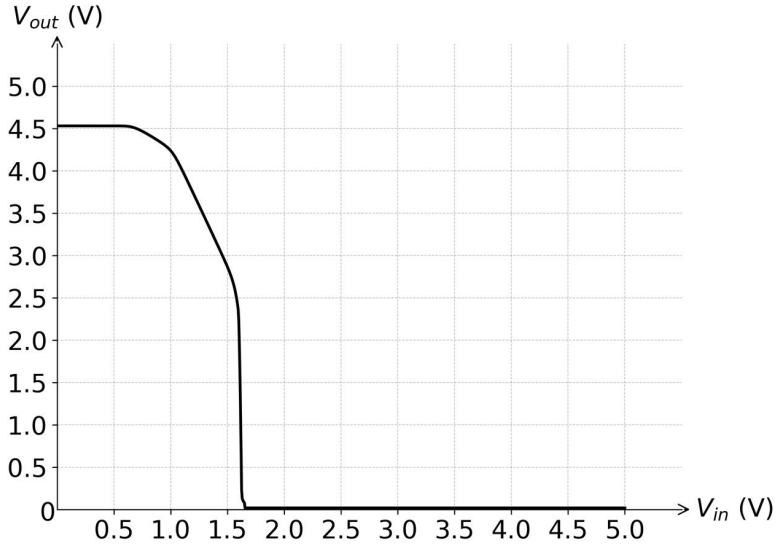

Fig. 4

(i) Estimate the high and low noise margins graphically. [12%]

(ii) Explain whether it is likely that the inverter characterised by Fig. 4 is implemented by the CMOS technology or not. [8%]

(b) A CMOS inverter is constructed with an NMOS transistor and a PMOS transistor, as shown in Fig. 5. Its output is loaded with a capacitor C_L.

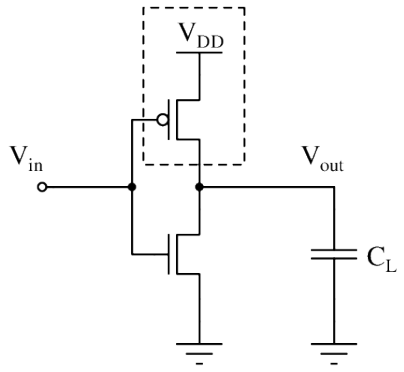

Fig. 5

(i) Sketch the cross-sectional device structure of the PMOS transistor that is inside the dashed region in Fig. 5. Assume the inverter was fabricated in the conventional

twin-well process. Based on your sketch, discuss the mode of operation of the transistor when input $V_{in} = V_{DD}/2$. State your assumption(s). [30%]

(ii) Explain the effect of the ratio between the widths of the PMOS transistor and the NMOS transistor on the voltage transfer characteristics (VTC) of the inverter. [20%]

(iii) If C_L = 125 pF is initially charged to V_{DD} = 1.8 V, the width of the NMOS transistor W_n = 200 nm, the width of the PMOS transistor W_p = 300 nm and the lengths of both transistors $L_n = L_p$ = 180 nm, calculate the fall time t_f for the output. State your assumptions. [30%]

You may find the constants in Table 1 and equations below useful.

	NMOS	**PMOS**
Critical field (E_C)	6×10^4 V cm^{-1}	24×10^4 V cm^{-1}
Effective Mobility (μ_e)	270 cm^2 V^{-1} s^{-1}	70 cm^2 V^{-1} s^{-1}
Threshold Voltage (V_T)	0.5 V	−0.5 V
Oxide Capacitance (C_{ox})	1.0 μF cm^{-2}	
Carrier Saturation Velocity (υ_{sat})	8×10^6 cm s^{-1}	

Table 1

$$V_{DSAT} = \frac{(V_{GS} - V_T)E_C L}{(V_{GS} - V_T) + E_C L}$$

$$I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_C L}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}, \qquad \text{for} \quad V_{DS} < V_{DSAT}$$

$$I_{DS} = W\upsilon_{sat}C_{ox}\frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_C L}, \qquad \text{for} \quad V_{DS} \geq V_{DSAT}$$

$$R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{Dsat}}$$

4 (a) You are given a Boolean function $F = A\overline{B} + A\overline{C}$.

(i) Design a CMOS gate for F with as few transistors as possible. Draw the transistor schematic. Use only positive input phases A, B and C. [20%]

(ii) Identify and explain a particular input combination that gives the longest propagation delay of your design in part (i). You may assume that all three inputs switch at the same time. [15%]

(b) Analyse the CMOS implementation of a clocked J-K bistable in Fig. 6 and explain its working principle. Give a reason for the unpopularity of such design in modern integrated electronics. The excitation table for the J-K bistable is given in Table 2. [35%]

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Table 2

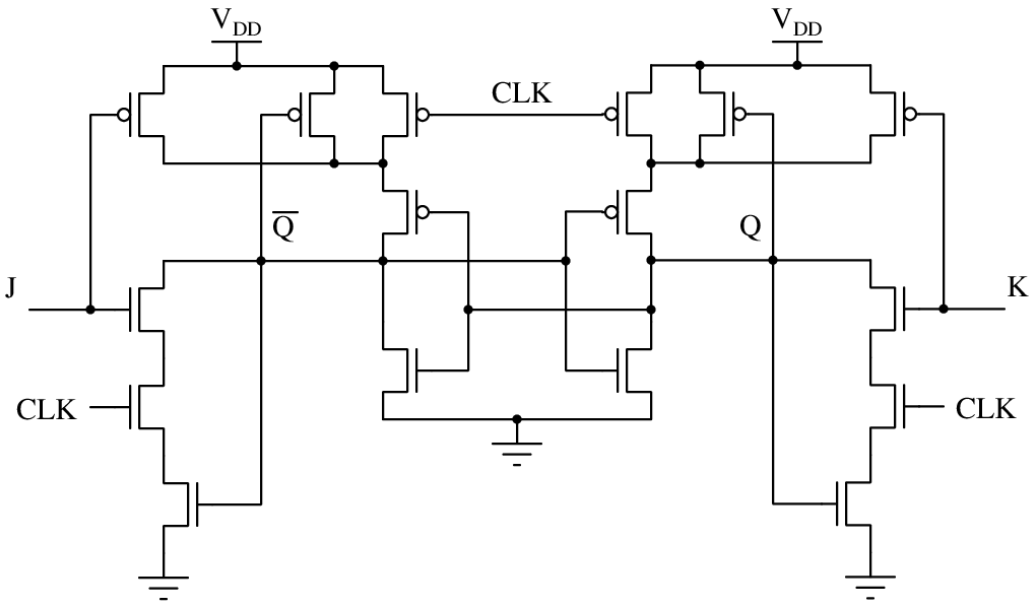

Fig. 6

(c) Fig. 7 shows the typical implementation of the static random access memory (SRAM) cell.

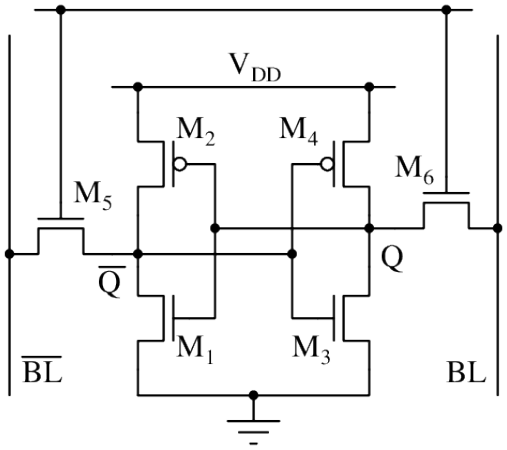

Fig. 7

(i) Explain the procedure to write logic '1' to the cell with reference to Fig. 7. [15%]

(ii) Transistor scaling leads to higher power dissipation. Suggest how FinFET could mitigate this problem. [15%]

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