Version SMG/5

EGT2
ENGINEERING TRIPOS PART IIA

Thursday 8 May 2025 9.30 to 11.10

Module 3B3

SWITCHED-MODE POWER ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) The circuit in Fig. 1 converts a DC input voltage V_{in} into a different DC voltage V_{out}. T_{on} is the time interval in each switching period during which the transistor is turned on. $f = 1/T$ is the switching frequency. How many switching states does the circuit have? Sketch an equivalent circuit for each state. [10%]

(b) Derive the output voltage V_{out} as a function of the input voltage V_{in}. Define a duty cycle with the above-given variables and assume the transistors and diodes are ideal and that the input current never ceases. Please state any other assumptions. [10%]

(c) How is the mode called in which this converter is operated with the above given conditions? Calculate the required duty cycle range if the circuit is part of a power bank and should deliver a constant voltage of 5 V to a USB connector from a specific lithium-ion battery, which delivers 4.2 V when full and 2.3 V when close to empty. [20%]

(d) Find the minimum of the inductance value L for a switching frequency of $f = 100$ kHz so that the circuit can reach 20 W output power in the entire operating range. [20%]

(e) Carefully sketch the inductor current as well as the inductor voltage, the input current and input voltage, and the output voltage over time at the operating point that determines the minimum inductance. Calculate the maximum and minimum levels of the inductor voltage. Clearly indicate which curve is which and label all axes. Furthermore, add as dashed lines the equivalent curves for smaller values of the inductance L. Which other parameter would have to change for a smaller L if the output voltage should remain at 5 V? [20%]

(f) Which change is required to use this circuit practically if that meant that the circuit would need to charge the internal battery through the very same USB port that is connected to the output capacitor? How would the replaced devices need to be operated? Sketch the modified circuit. Which other advantages would this modification entail for the overall circuit when the real, non-ideal behaviour of components is considered? Further discuss why designers often keep the battery voltage below the output voltage and use this type of circuit for the conversion. You might find it useful to refer to the current traces of part (e). [20%]

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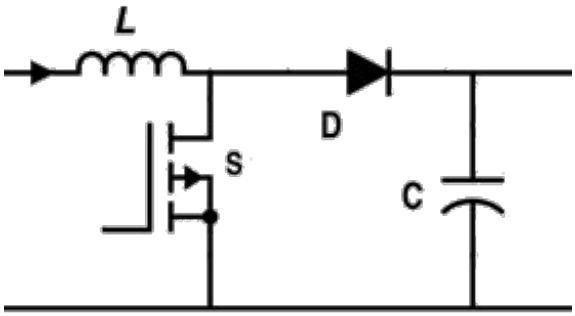

Fig. 1

2 (a) A single-phase bridge rectifier connected to 230 V, 50 Hz supplies a constant current to a load. The output voltage is smoothed by a capacitor. The load can be represented by a resistor. Sketch the circuit. [15%]

(b) Derive an expression for the output voltage ripple and state your assumptions. Furthermore, choose a value for the resistor and the capacitor such that the average load current is 20 A and the voltage ripple 5%. [20%]

(c) Sketch the real voltages and currents over time at the input and the output without simplifications. Explain why the circuit is problematic and in which way. [30%]

(d) How can the circuit be modified to avoid the problem from part (c) but still have low voltage ripple at the output? Sketch the new voltages and currents over time at the input and the output. Compare the traces with the case in which the rectifier is connected directly to a linear resistor only without any other element. [35%]

3 A smart mobile phone charger comprises a single-phase diode-bridge rectifier and a MOSFET-based Flyback DC-DC converter. The input voltage is 230 V and the output is 15 V. The MOSFET is operated at 500 kHz. The load current is 2 A. The magnetic core of the Flyback converter has a cross section area of 0.25 cm^2 and saturates at a flux density of 0.36 T. The flux in the transformer is critically continuous and the peak is at least 25% below the saturation point. The duty cyle of this Flyback converter is limited to 50%. Components in this converter are considered as ideal and the converter is lossless.

(a) Sketch the circuit schematic of the charger. Explain the necessity of using the Flyback converter instead of a Buck converter. [15%]

(b) When the duty cycle is 50%, sketch the waveforms of the MOSFET voltage, the MOSFET current, the diode current, and the magnetic flux of the Flyback converter against time. [20%]

(c) Calculate the number of turns of each winding of the transformer in the Flyback converter. Calculate the adjusted duty cycle when the output is kept at 15 V. [25%]

(d) Calculate the effective relative permeability of the core when the effective length of the core is 2 cm. The permeability of free space is 1.26×10^{-6} H/m. [20%]

(e) Explain why the flux of the transformer is preferably critically continuous for the Flyback converter. How should the transformer core setting be adjusted if the load current is doubled? [20%]

4 Two MOSFETs are used in a synchronised Boost converter as shown in Fig. 2. The switching frequency is 100 kHz and the output voltage V_o is 100 V. The synchronised Boost converter operates in the Continuous Conduction Mode (CCM) and the duty cycle is 75%. The input power is 250 W and the inductor L has a 40% peak-to-peak current ripple.

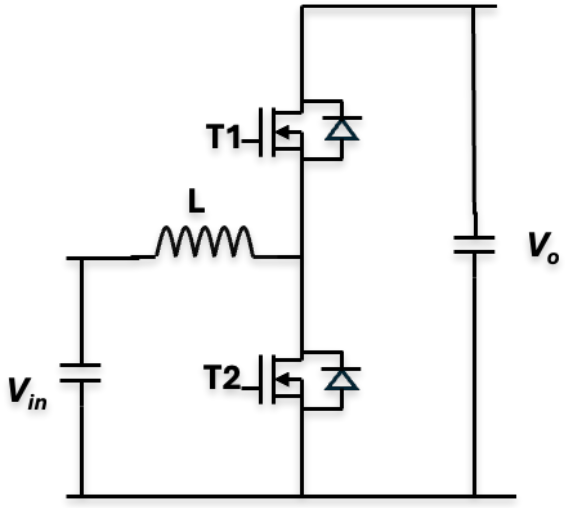

Fig. 2

(a) What is the dead time? Explain the necessity of the dead time. [15%]

(b) Calculate the conduction loss of MOSFET T2. The on-state equivalent resistance of the MOSFET R_{DS} in this converter is 50 mΩ. [20%]

(c) Sketch the simplified curve of the gate to source voltage V_{GS}, gate current I_G, drain-to-source voltage V_{DS}, and drain current I_D of MOSFET T2 for the switch-on and switch-off events, respectively. Mark the switch-on delay time t_{don}, switch-on rise time t_r, switch-off delay time t_{doff}, and switch-off fall time t_f. [25%]

(d) Calculate the switching loss of MOSFET T2 when t_{don} is 14 ns and t_r is 16 ns. Assume that the switch-off loss equals the switch-on loss. [20%]

(e) Sketch the current commutating loops in one switching period. Explain why MOSFET T2 has a larger switching loss than MOSFET T1. [20%]

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