Answers 4B2 - 2026

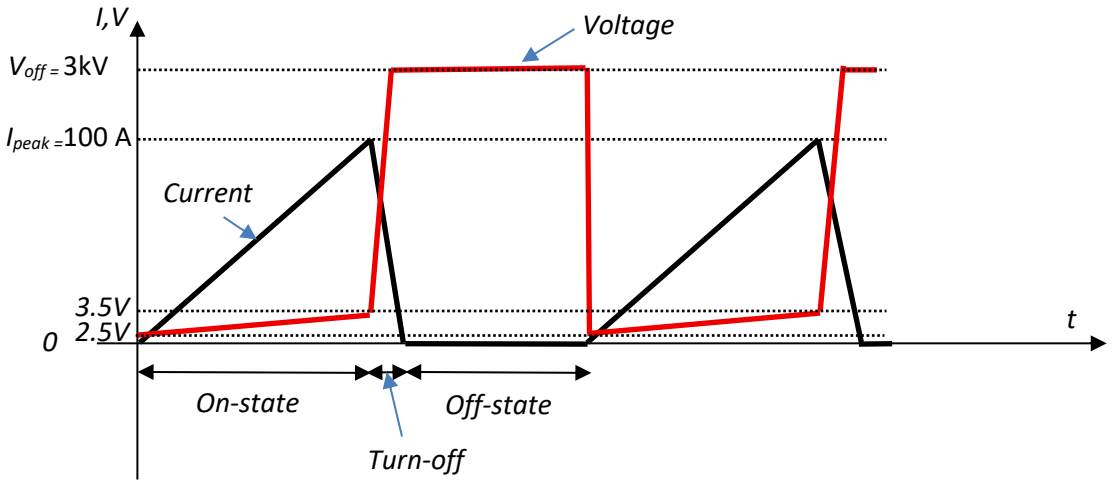
1 (a) Typical AlGaN thicknesses in high voltage GaN HEMTs are 10-20nm. Increasing the AlGaN layer would increase the polarization and therefore will make the piezo-polarization charge (and therefore the 2DEG charge density) at the Gan/AlGan interface stronger. This would lead to a lower on-state resistance. High 2DEG densities however would result in lower 2DEG mobility (due to carrier-to-carrier scattering) which unfortunately counteracts to some extent for the increase in the charge density level, leading to a less positive effect on the on-state resistance. Moreover, as the AlGaN thickness is increased, the depletion of the 2DEG becomes more difficult and therefore the device may exhibit a lower breakdown voltage and a lower threshold voltage (threshold voltage can become negative too, leading to a normally-on device). This is a disadvantage as a relatively large threshold voltage (in excess of 1.5V) is desirable to avoid the parasitic re-triggering of the transistor in the on-state while switching off large dV/dt currents. [20%]

1b (i). $V_{on\text{-}peak} = V_{offset} + R\, I_{peak} = 2.5 + 0.01x100 = 3.5\ V$

Define $\alpha = \frac{I_{peak}}{DT}$ the slope of the current growth in time,

$P_{ON} = \frac{1}{T}\int_0^{DT} V_{ON} I_{ON} dt = \frac{1}{T}\int_0^{DT} \alpha t \left[V_{offset} + R\alpha t\right] dt = \frac{1}{T}\int_0^{DT} \left(\frac{I_{peak}}{DT}\right) V_{offset} t\, dt\ +$
$\frac{1}{T}\int_0^{DT} \left(\frac{I_{peak}}{DT}\right)^2 R t^2 dt + = \frac{I_{peak} V_{offset}}{2} D + \frac{{I_{peak}}^2 R}{3} D \quad = \frac{100\ x2.5}{2}\ 0.5 + \frac{100^2\ x0.01}{3}\ 0.5 = 62.5W\ +$
$16.67W = 79.17W$

One can note that the largest on-state losses are associated with the on-state offset voltage rather than associated with the equivalent resistance R. ,



[50%]

(ii) The switching losses can be calculated simply as the product between the switching energy per switching cycle and the frequency. The switching losses are only made of turn-off losses. The total $Ps_{witching} = f\ E_{sw\text{-}cycle} = 150W$.

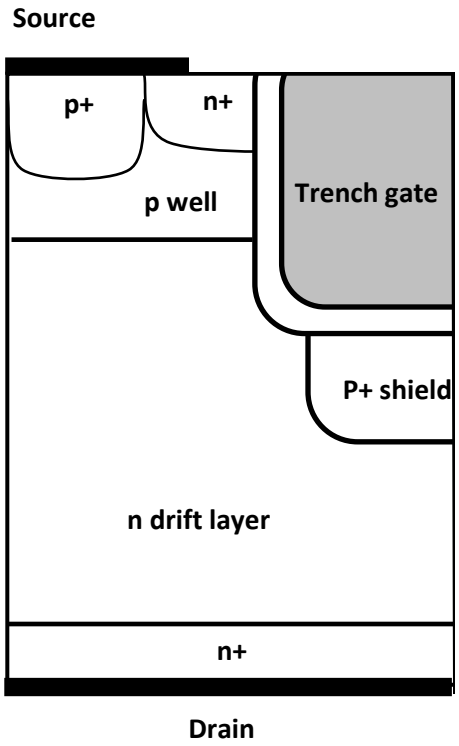
The switching loses are ~ twice the on-state losses. For a balanced system, the switching frequency could be reduced to 25 kHz, to ensure that on-state losses are ~ equal to switching losses. This would improve efficiency while still delivering reasonable form factor for the passives in the power electronics system. [15%]

(iii). There are multiple sources of errors. During on-state the temperature does not stay constant, as the device self-heats. In general IGBTs change from a negative temperature coefficient at low currents to a positive temperature coefficient at high currents. The simple linear relationship given by eq (1) does not capture this behaviour. Nor it captures the conductivity modulation of the drift region which has a super-linear curve.

The offset voltage is very high (2.5V) indicating that the IGBT is built in a wide bandgap semiconductor (Silicon Carbide or Gallium Nitride). This is because the built-in potential of a Silicon Carbide or Gallium nitride junction is ~ 2.3-2.5V. Between the two materials, Silicon Carbide (SiC) would be the preferred choice as GaN has very low lifetime (due to defects) and the conductivity modulation due to bipolar injection would be insignificant.

The losses associated with the offset voltage (2.5V) are the dominant contribution in the on-state losses (see point (i)). This is one of the reason that <u>silicon</u> IGBTs are very successful and popular while <u>SiC</u> IGBTs should only be considered for extremely high voltage applications (eg. 10KV and above). [15%]

2. (a)



The p+ is connected to the source terminal in the third dimension (not shown). The main purposes of the p+ shield are :

(i) to protect the gate oxide against high electric fields from the drain. This would lower the tunnelling current to the gate when high voltages are present on the drain, but also make the device more reliable against static and dynamic dielectric breakdown.

(ii) Lower the Cgd (Miller) capacitance. The p+ should will cause an additional depletion capacitance in series with gate capacitance. The p+ will also be connected to the source terminal.

(iii) Protect the corner of the trench against high electric fields.

On-state: The p+ shield will introduce a JFET effect (obstruction of current due to depletion regions) which can cause a higher on-state resistance. To counteract this a more highly n-type doped layer should be added just below the p well.

Off-state: The shield would allow a lower electric field at the corner of the trench resulting in enhanced breakdown and reliability.

Turn-on and turn-off. The presence of the shield would lower the Cgd and introduce a faster depletion in the n drift. As a result the losses during the transients would be smaller, [35%]

(b) (i) **Over current Sensing and Protection.** The sense IGBT has an identical structure to the main IGBT, but a fraction of the active area. The Sense IGBT takes a known fraction of the current (say 100x less) of the main IGBT. By measuring the current in the Sense IGBT, the current in the IGBT could be calculated. The current in the Sense IGBT (and hence in the main IGBT) is measured by the voltage drop on the resistor R1 (sensing) When the voltage drop on R1 exceeds the threshold voltage of the MOSFET M1 , then M1 is turned off and pulls down the gate of the main IGBT, thus lowering the current on the IGBT (protection function).

Over voltage sensing and protection. The avalanche diode DAval becomes active during the blocking mode. DAval is designed to break down just before the IGBT breaks down. When the avalanche diode breaks down the gate of the IGBT is pulled up, thus turning on the main IGBT. The avalanche current is then spread over a large area (rather than being concentrated in a spot), thus allowing higher avalanche current to be supported during the breakdown. The idea is to avoid thermal failure due to localised avalanche.

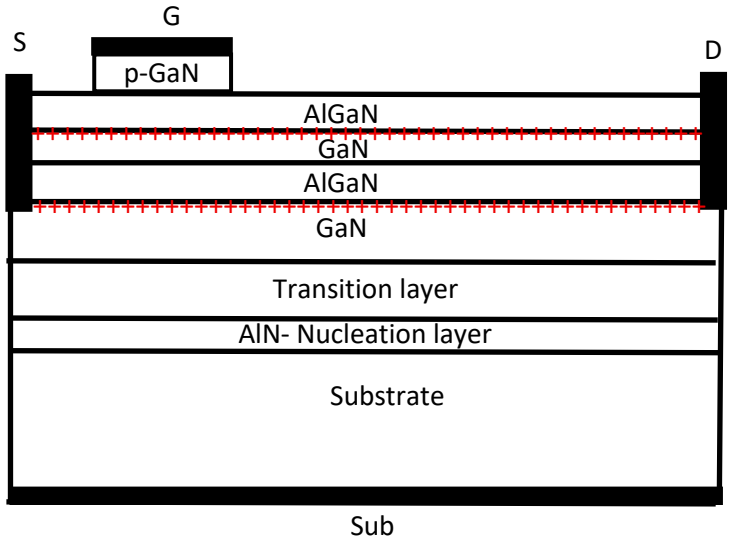
Over temperature sensing and protection. S1 to Sn are thermal diodes. They are operated in forward bias and biased with a constant current supplied by the current mirror made with M3, M4 and Rref. Rref adjusts the current level. The voltage drop in each of the thermal diodes, decreases lineally with temperature with approx. -2mv/C. The diodes are put in series to increase the total voltage drop across them. When the temperature in the device reaches a certain level (designed to be slightly less than the junction temperature) – say 170C, the voltage drop on the series D11 and Dsn reduces thus pulling up the gate of M2. If M2 turns on, the gate on the main IGBT is pulled down, thus reducing the current in the main IGBT and hence lowering the temperature.

RG adjusts the delay in the turn-off and modulates the dV/dt. D1 prevents the forward bias of DAval. [50%]#

(c) The Sense IGBT should have an identical structure and design to the main IGBT, except that has much smaller active area (say 100X smaller). There are two possible issues concerning the scaling of the current in the Sense IGBT compared to the Main IGBT: (i) Because of the voltage R1, both the Vds and the effective Vgs in the sense IGBT are smaller than in the main IGBT. Thus the scaling of the current is not perfect. The Sense IGBT will enter saturation earlier than the main IGBT. (ii) the temperature in the sense IGBT could be different than in the main IGBT – because of the power dissipation being different but also because of different placement within the smart chip. [15%]

3. (a)

The piezo-polarization charge is placed at the interfaces between GaN (bottom) and AlGaN (top). This charge is positive and is compensated by a 2DEG (confined – quantum - gas of electrons) negative charge. There are two channels in this case from source to drain. The positive piezo-polarization charge (positive) is indicated below (in red colour). [Note that there is also a negative piezo-polarization charge (which could attract holes) at the AlGaN (bottom)/GaN (top) interface. The amount of holes could be very little and their mobility is very low – for this reason we neglect their contributions.]



On-state: the electron current flows from source to drain and is modulated by the gate-source voltage drop. When the gate-source voltage drop is less than a threshold the current stops. The higher this voltage drop, the higher the electron charge in the two channels and the lower the on-state resistance. Saturation of the current happens when the electron velocity saturates in both channels.

Note that the upper channel is more effectively modulated by the gate voltage while the lower channel is not. The device is normally-on, as even if the first channel is depleted when the gate-source voltage is zero volts, the second channel is not. The second channel can only be depleted when the depletion region from the p GaN reaches both the channels. This is likely to be a very negative gate voltage depending on the thickness of the GaN/AlGaN layers and the mole fraction

Off-state: Gate-source voltage I below the threshold voltage. Both channels are depleted and the off-state voltage is supported within the gate-to-drain space. The second channel is

delaying the advance of the depletion region towards the drain, putting more field pressure on the gate structure. This could result in reliability – dynamic Ron problems – and lower breakdown.

Turn-on and turn-off are achieved by increasing the gate-to-source voltage above the threshold voltage and by lowering it below the threshold respectively. Given the low form factor (because of the very low specific on-0state resistance) the capacitances are low and the device switches very fast. [55%]

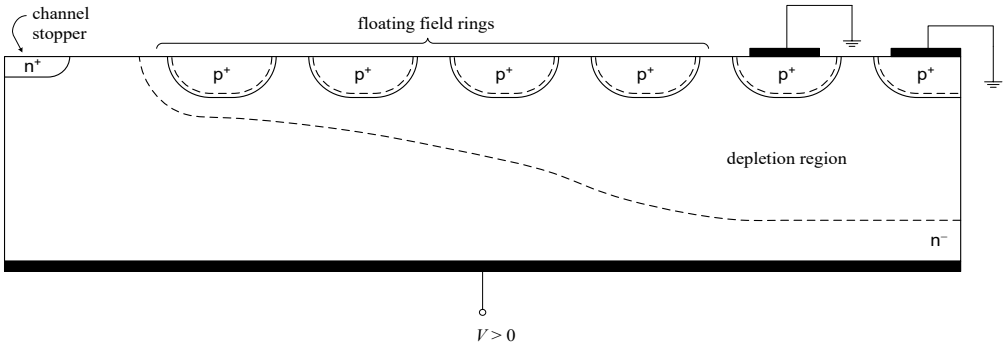
(b) Advantage: lower specific on-state resistance due to the additional presence of the second 2DEG channel
Disadvantages: (i) normally-on device, difficult to control the threshold voltage (ii) higher field pressure at the gate side leading to reliability issues and lower breakdown (iii) complex fabrication and higher cost. [15%]

(c) The sub terminal should be connected to source or to the lowest potential to avoid excessive leakage through the substrate. Changing the substrate from silicon to silicon carbide (Sic) can have major advantages such as high thermal conductivity (meaning that the device will self-heat less) and very good lattice match to the GaN layers above. This means that there will be no need for the transition later reducing the epi-stack and lowering the GaN epi cost. However SiC wafers are much less common and considerably more expensive. [15%]

(d) The Schottky gate is used for normally-on devices in classical GaN technology. Here, changing from p-GaN to a Schottky means that the threshold voltage will become even more negative, possibly un-usable in practice. This would exacerbate the disadvantage of this device compared to a classical HEMT. [15%]

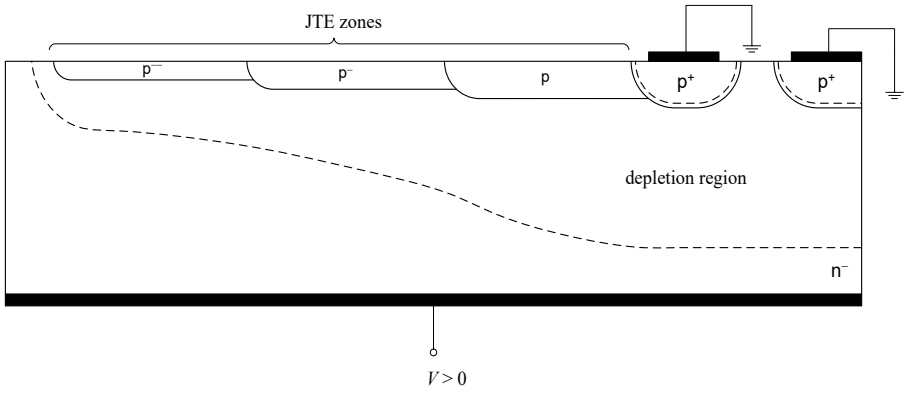
4. (a) The shape of the junction which supports the voltage plays an important role in ‘field crowding’. The higher the radius of a cylindrical or spherical junction the closer the breakdown is to that of an ideal parallel-plane junction. However, in most microelectronics processes the junction depth is limited to a couple of microns up to maximum 10-15 microns. The curvature effect can be reduced in multiple cell power devices such as MOSFETs or IGBTs by placing the cells (with multiple junctions) close together to simulate almost a ‘continuous junction’. Field plates can also be used to reduce the curvature effect.

Floating Rings
The use of multiple floating rings (concentric highly doped p+ rings surrounding the active area of the device). The idea is to gradually release the depletion region at the edge of the device. The voltage is supported between each pair of p+ rings thus reducing the crowding of the electric field at the surface. The spacing and depth of the rings are designed such that the electric field peaks at the surface between each pair of rings are almost equal and the breakdown voltage of the final structure is at least 90% of the bulk breakdown.



Junction Termination Extension (JTE)

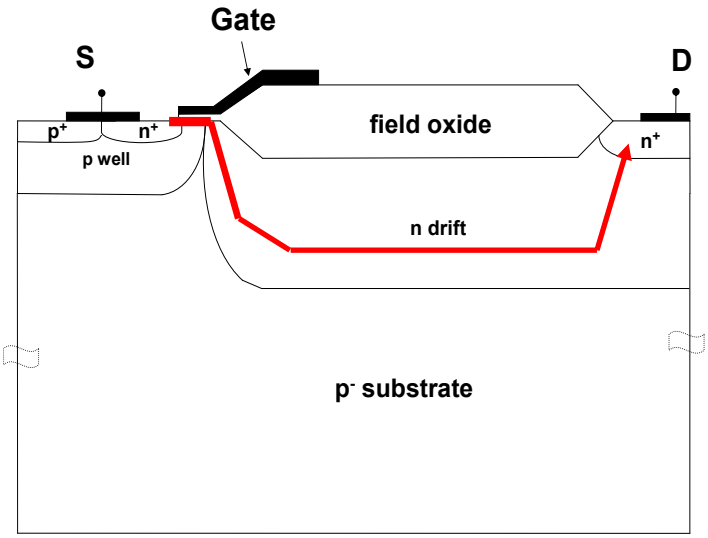
Use of multiple zones with the doping level decreasing from the active area towards the end of the termination. The effect is similar to that achieved by the field rings – that is the gradual release of the depletion region at the edge of the device. The voltage is ideally supported uniformly along the JTE zones.



[35%]

(b) The field rings that are closer to the active area have a smaller equivalent radius of a spherical (or cylindrical) junction when compared to the field rings that are farther away from the active area. Therefore to avoid high electric fields next to the active area, the inner rings should have a smaller distance between them. Hence they absorb a smaller voltage between them compared to the outer rings. A good optimisation is when all the electric field peaks between the rings are equal at breakdown so the device theoretically breaks in all points at the same time. This would lead to the maximum efficiency of breakdown per unit area. For this the distance between the rings should be increased gradually from the first ring (i.e. the ring that is the closest to the active cell) to the last ring (the farthest from the active cell). [20%]

(c) The Resurf LDMOSFET is a classical device in silicon technologies. Its use is in the 100V to 600V voltage class. For the 600V class the power is limited to tens of Watts (relatively low power applications).



The advantages of the lateral technology in silicon is that intelligent (mix mode – analogue ad/or digital) circuits can be integrated monolithically alongside the LDMOSFET. within the same chip. This is not case in vertical technologies. Because of the low critical electric field in silicon (0.3 MV/cm) the distance between the gate and drain needs to be increased (e.g. 60 um for a 600 V device) limiting the current and power capability of this device. The insulated gate is made of silicon dioxide, and it offers an excellent interface to silicon. The bulk and channel electron mobilities are very high. The threshold voltage is stable and easily controllable by the surface doping of the p well.

In lateral technologies the gate density is relatively low (compared to vertical technologies). If this device were to be made in silicon Carbide, the channel mobility would be very low and because of the low density of gates, the channel resistance would be very high. Intelligence in SiC can be done but the performance would be very poor. The p-channel SiC mobilities are extremely poor. This is why only vertical technologies have been successful in SiC (and over 600V). In GaN, the insulated gate is very unstable and affected by traps. This technology offers no advantages over the lateral HEMT. The lateral HEMT additionally benefits from very 2DEG mobilities and high piezo-polarization charge. [25%]

(d) at 600V,

(i) Advantage: GaN HEMT has higher mobility (2000 $cm^2/(Vs)$) and much lower capacitances. The very low channel mobility in SiC (20 $cm^2/(Vs)$) means that the gate density needs to be increased resulting in very high Cgs and Cgs capacitances, as well as high gate charge.
Advantage: GaN HEMT can have intelligence monolithically integrated
Disadvantage: GaN is a lateral device, the specific on-state resistance of the vertical SiC is smaller than that of GaN. The SiC chip can be smaller and can be more economical for the same on-resistance.

At 1.5kV the Gan would require a huge epi stack and the lateral technology becomes less efficient. This is the reason there are no GaN HEMTs at voltages above 1.2 kV [20%]