Version MWCT/5

EGT3
ENGINEERING TRIPOS PART IIB

Monday 5 May 2025 9.30 to 11.10

Module 4B28

VERY-LARGE SCALE INTEGRATION (VLSI)

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper.

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed.
Attachment: 4B28 Very-Large Scale Integration (VLSI) data sheet (4 pages).

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 The cross-section of a fabricated PMOS transistor is shown in Fig. 1.

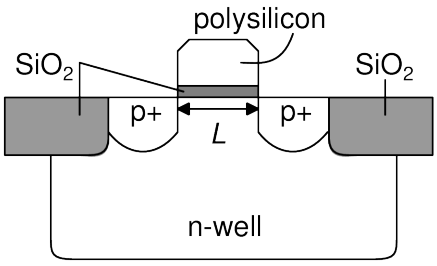

Fig. 1

(a) VLSI fabrication engineers have been trying to reduce the length L of CMOS transistors for years. Explain the most important reason behind the reduction of L. Moreover, discuss an effect of reduction in L on the electrical properties of the fabricated PMOS transistor. [20%]

(b) The gate-to-channel capacitance C_{GC} is affected by the mode of operations of the transistor. Based on the structure shown in Fig. 1, explain briefly the sources of C_{GC} when the transistor is cut-off and in saturation. [15%]

(c) If the transistor of length 0.2 μm was fabricated using the generic 0.18 μm technology to provide a 10 μA current from its source to its drain under the following operating conditions: $|V_{GSp}|$ = 0.8 V, $|V_{DSp}|$ = 0.4 V, $|V_{BSp}|$ = 0 V. What should be the width of this transistor, if the transistor is assumed to be a short-channel device? Ignore channel length modulation. [30%]

(d) Explain why a PMOS transistor is not an ideal switch. Discuss a CMOS circuit that could serve better as a switch for digital systems. [20%]

(e) An engineer said: "*the resistance of the PMOS transistor in the 0.18 μm generic technology is around 30 kΩ when its width and length are both 200 nm*". Explain whether you agree with this statement or not. [15%]

Numerical answers: (c) 0.7 μm

2 A three-variable Boolean function F is given as:

$$F = A(\overline{B} + \overline{C})$$

(a) Design a static CMOS gate for F and provide the size ratios for all transistors such that the *worse-case* pull-up and pull-down equivalent resistances of the gate is equivalent to that of the standard inverter. Assume that only positive phases of the variables (i.e. A, B and C) are available. Use no more than ten transistors and connect as many transistors to V_{DD} or GND as you can. [25%]

(b) If area is of utmost importance, what change(s) would you make to the static gate in part (a)? Explain one trade-off for such change(s). [15%]

(c) Show that the logical effort g for the input B of the static gate in part (a) is 2. Thus, derive the *worse-case* intrinsic delay p. [20%]

(d) Using the logic gate for F as an example, explain the two sources of dynamic power in static CMOS gates. [20%]

(e) Suppose the logic gate X is used in a multi-level digital circuit shown in Fig. 2. The inverter is of the standard size, the 2-input NAND gates are of the same size, and it is given that the input capacitance to the inverter and the final load capacitance are 3 fF and 20 fF respectively. Assume that the ratio between the gate input capacitance and the gate intrinsic capacitance $\gamma = \dfrac{C_g}{C_{int}}$ is 1.

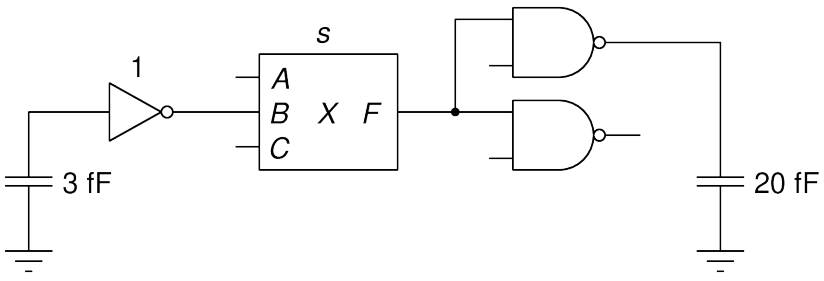

Fig. 2

Based on the logical effort method, determine the size ratio s for X that would minimise the propagation delay to drive the load. [20%]

Numerical answers: (c) $\frac{10}{3}$ (e) 3.29

3 A clock distribution network with a clock source S and five sink nodes A, B, C, D and E was routed on metal tracks with a pitch of 1 mm. Fig. 3 shows the network. The width of metal interconnect is 2 μm, and the sheet resistance of the metal is 5 m$\Omega/\square$. It is known that the sink nodes all have a lumped capacitance of 80 fF.

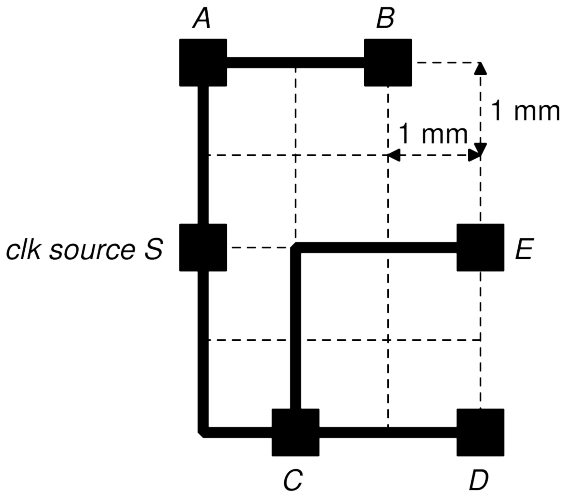

Fig. 3

(a) Calculate the resistance of an interconnect segment of 1 mm length. Using this result, sketch the resistor-capacitor (RC) tree modelled from the clock distribution network in Fig. 3. [30%]

(b) Thus, calculate Elmore delays τ_B and τ_E at nodes B and E respectively. [20%]

(c) How does the difference in arrival times of the clock signals affect the clock frequency to operate the system? Discuss a measure to mitigate the difference. [15%]

(d) Fig. 4 illustrates the design of a dynamic, true single-phase clock register. Assume that all transistors had been carefully sized to ensure correct function. Explain the working principle of this positive-edge triggered register. [20%]

(e) Explain whether the register in Fig. 4 is suitable for the clock distribution network in Fig. 3 or not. Assume a perfect clock source at S. [15%]

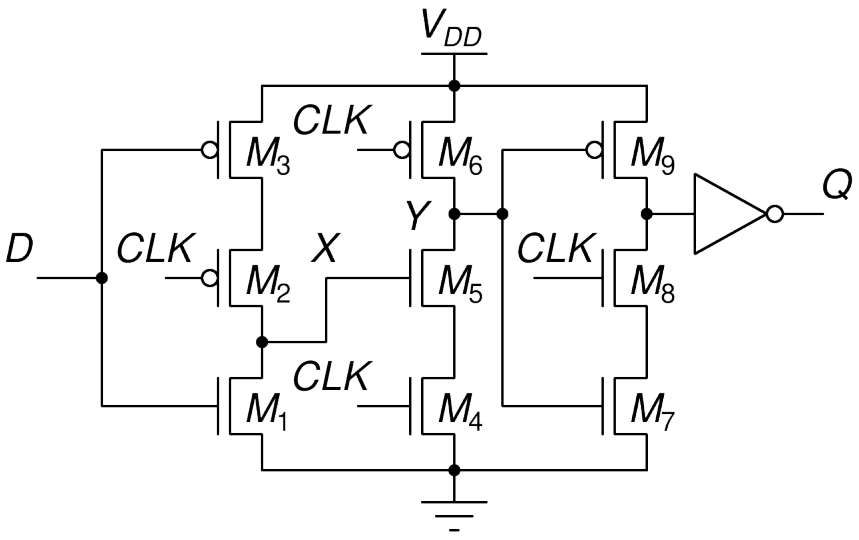

Fig. 4

Numerical answers: (a) 2.5 Ω (b) 1.2 ps; 2.6 ps

4 Fig. 5 shows a dynamic XNOR gate in the generic 0.13 μm technology with input arriving in both positive and negative phases. The lengths and widths of all NMOS transistors are 100 nm and 300 nm respectively.

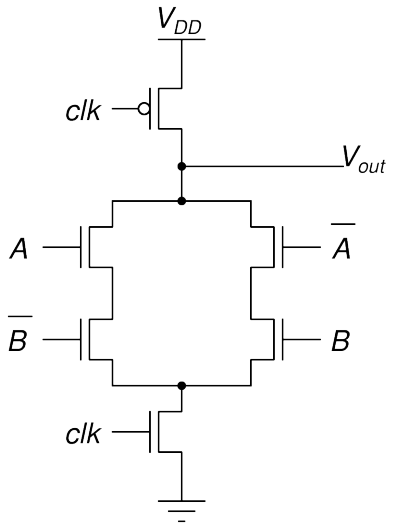

Fig. 5

(a) Calculate the equivalent pull-down resistance of the gate. [15%]

(b) Derive the logical effort for this gate when the gate output is 0. Assume that every input (A, $\overline{A}$, B, $\overline{B}$) is provided independently. [15%]

(c) From the measurement of a fabricated gate, the output voltage V_{out} gradually drops during the evaluation phase, even when the output should be 1 and is not connected to any other gate. Explain this phenomenon. Will the voltage drop increase or decrease as the VLSI technology scales down (i.e. smaller feature size)? [25%]

(d) Discuss a potential issue when cascading this dynamic gate. Propose a solution for the issue. [25%]

(e) Design an alternative gate for the same XNOR function but with fewer transistors. State a disadvantage of your alternative design when compared with the dynamic gate. [20%]

Numerical answers: (a) 12.5 kΩ (b) 1

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