Version MWCT/3

EGT3
ENGINEERING TRIPOS PART IIB

Tuesday 5 May 2026 9.30 to 11.10

Module 4B28

VERY LARGE SCALE INTEGRATION (VLSI)

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Attachment: 4B28 Very Large Scale Integration (VLSI) data sheet (4 pages)

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Discuss how process variations in widths and lengths of transistors affects the robustness and performance of a CMOS inverter. [25%]

(b) A CMOS inverter fabricated in the generic 0.18 μm technology is shown in Fig. 1. The widths of the NMOS and PMOS are 400 nm and 280 nm respectively, and the lengths of the transistors are both 200 nm. There is a capacitive load of 25 pF at its output.

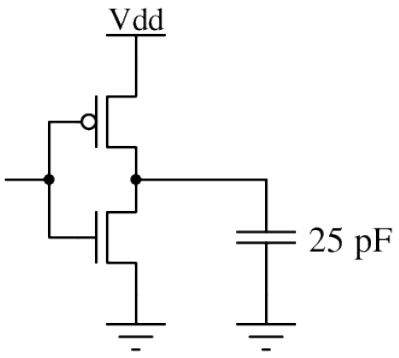


Fig. 1

(i) Estimate the switching threshold V_M of the CMOS inverter. [10%]

(ii) Hence, estimate the maximum instantaneous power of the inverter. [20%]

(iii) Assume a step input from high to low, estimate the propagation delay. State your assumption. [15%]

(c) Explain two issues associated with using a single PMOS transistor as a switch. Then, design an OR gate using PMOS pass transistors. Assume both polarities of the input variables A, B, $\overline{A}$ and $\overline{B}$ are available. [30%]

2 Figure 2 shows the typical cross-sectional structure of a *deep-trench* dynamic random access memory (DRAM) cell, fabricated on silicon substrate.

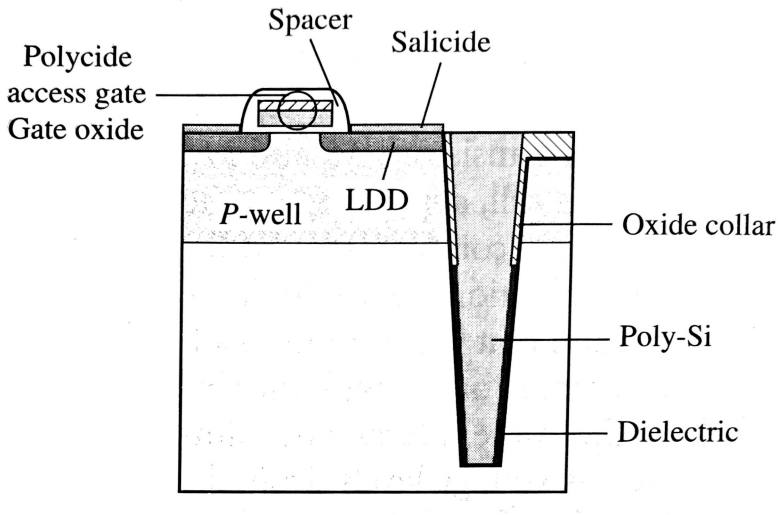


Fig. 2

(a) Describe how the trench could be fabricated using photolithography. Assume that previous layers had been fabricated perfectly. [25%]

(b) Draw a labelled circuit schematic for a DRAM cell. [20%]

(c) The length and width of the bitline (BL), which is routed on the first aluminum layer (Al1), is 500 μm and 400 nm respectively. The sheet resistance at this layer is 0.1 $\Omega\,\square^{-1}$.

(i) Estimate its lumped resistance and capacitance, assuming that the interconnect is entirely over active transistor area. Ignore the effect of inter-wire capacitance. [20%]

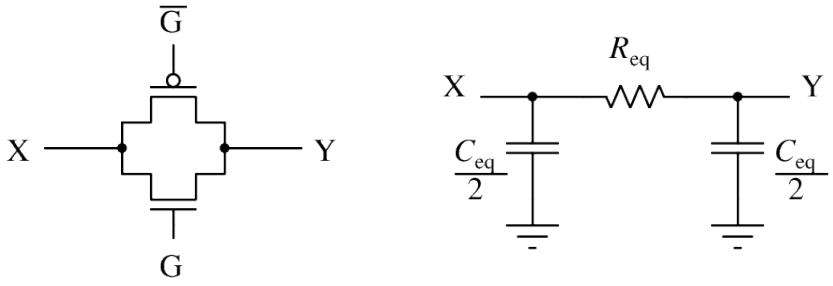
(ii) The DRAM cell storage capacitance C_S is measured as 20 pF. The sensing requirement on the bitline BL is ΔV = 80 mV, which is given by the equation:

$$\Delta V = V_{BL} - V_{BLP} = (V_{cell} - V_{BLP})\frac{C_S}{C_S + C_{BL}}$$

Suggest appropriate operating voltages for precharge, bitline V_{BLP} and cell storage V_{cell}. [15%]

(d) Account for key sources of power dissipations around the DRAM cell. [20%]

3 Figure 3(a) and (b) shows a transmission gate and its equivalent π-model respectively.



(a) Transmission gate (b) π -model

Fig. 3

(a) What is the primary source of parasitic capacitance for the transmission gate at points X and Y? Explain how you would estimate the equivalent resistance R_{eq} when it is turned on with $V_G = V_{DD}$. [25%]

(b) Consider the circuit constructed with a number of identical transmission gates in Fig. 4.

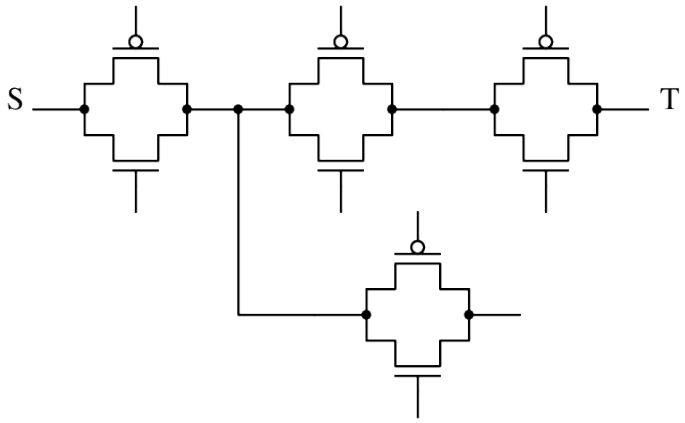


Fig. 4

Now given that R_{eq} = 35 kΩ and C_{eq} = 30 pF, calculate the Elmore delay at T by sketching an equivalent RC tree for the circuit. Assume a step input at S. [30%]

(c) Transmission gates can be used to build a two-stage positive-edge triggered flip-flop with synchronous reset, as illustrated in Fig. 5.

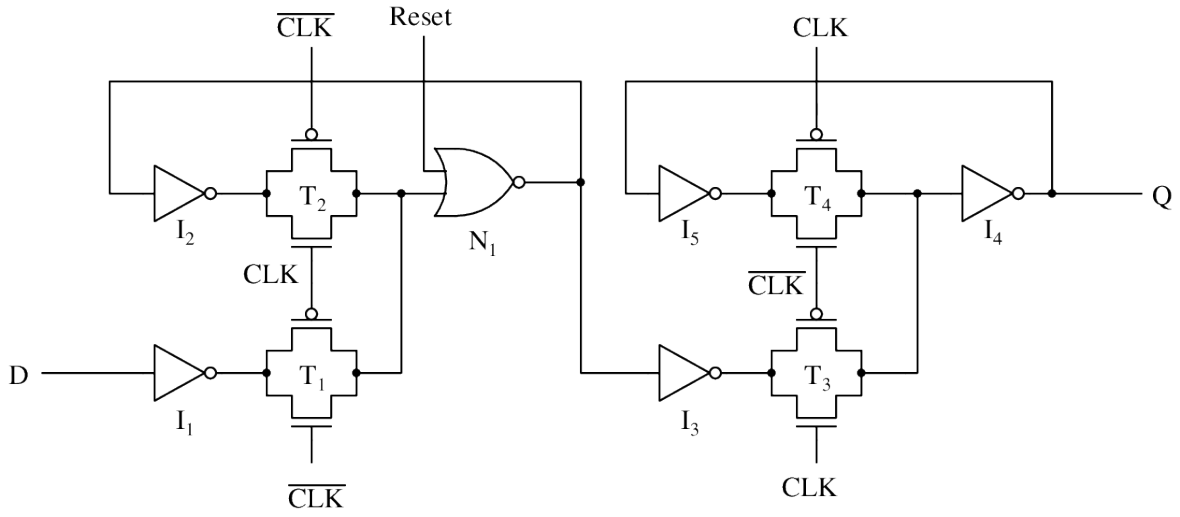


Fig. 5

(i) Estimate the number of transistors required for this circuit. [15%]

(ii) Derive, with explanation, the expression for setup time, hold time and propagation delay of this flip-flop in terms of the propagation delays of the inverters (d_{inv}), NOR gate (d_{nor}) and transmission gates (d_{tg}). [30%]

4 (a) Design a multi-stage OR gate with 32-bit input. The output of the gate has to drive a load of capacitance 2026 times larger than that of the input of the minimum size standard inverter.

(i) What would be an ideal number of stages N for the designed circuit? Justify the choice using the logical effort method. [20%]

(ii) Based on the choice in (i), sketch the logic path of the designed circuit and work out the sizes of all logic gates [25%]

(b) Design a *domino* OR gate $F = A + B + C$. Assume only the positive phase of the inputs A, B and C are available. Discuss why the domino gate is considerably faster than its static CMOS counterpart. [30%]

(c) Explain the impact of significant skew in the precharge/evaluation clock signal to the reliability of a system built by domino gates. [25%]

END OF PAPER

UNIVERSITY OF CAMBRIDGE | Department of Engineering

Part IIB - 4B28
Very Large Scale Integration (VLSI)
DATASHEET

Design parameters

		0.18 μm		0.13 μm		
Name	Symbol	NMOS	PMOS	NMOS	PMOS	Units
Channel Length	L	200	200	100	100	nm
Supply Voltage	V_{DD}	1.8	1.8	1.2	1.2	V
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	μF cm^{-2}
Threshold Voltage	V_{T0}	0.5	-0.5	0.4	-0.4	V
Body-Effect Term	γ	0.3	0.3	0.2	0.2	V$^{1/2}$
Fermi Potential	$2\lvert\phi_F\rvert$	0.84	0.84	0.88	0.88	V
Junction Capacitance Coefficient	C_{j0}	1.6	1.6	1.6	1.6	fF cm^{-2}
Built-in Junction Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Nominal Mobility (low vertical field)	μ_0	540	180	540	180	cm$^2V^{-1}s^{-1}$
Effective Mobility (high vertical field)	μ_e	270	70	270	70	cm$^2V^{-1}s^{-1}$
Critical Field	E_C	6×10^4	24×10^4	6×10^4	24×10^4	V cm^{-1}
Critical Field $\times L$	$E_C L$	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eq}	12.5	30	12.5	30	kΩ $\square^{-1}$

Threshold Voltage with Body Effect

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

Long-channel devices

$$V_{DS} < V_{GS} - V_T \qquad I_{DS} = \frac{W}{L}\frac{\mu_0 C_{ox}}{2}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \qquad \text{linear}$$

$$V_{DS} \geq V_{GS} - V_T \qquad I_{DS} = \frac{W}{L}\frac{\mu_0 C_{ox}}{2}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right) \qquad \text{saturation}$$

Velocity saturation short-channel devices

let $$V_{DSAT} = \frac{(V_{GS} - V_T)E_C L}{(V_{GS} - V_T) + E_C L}$$

$V_{DS} < V_{DSAT}$ $$I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_C L}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$ linear

$V_{DS} \geq V_{DSAT}$ $$I_{DS} = W v_{sat} C_{ox}\frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_C L}$$ saturation

Switching threshold V_M (short-channel device assumed)

$$V_M \approx \frac{V_{DD} - |V_{TP}| + rV_{TN}}{1 + r}$$

$$r = \sqrt{\frac{W_N/E_{CN}L_N}{W_P/E_{CP}L_P}} = \sqrt{\frac{W_N}{W_P}\cdot\frac{L_P}{L_N}\cdot\frac{E_{CP}}{E_{CN}}}$$

Transistor equivalent resistance

$$R = \frac{1}{2}\left(\frac{V_{DD}}{I_{Dsat}} + \frac{V_{DD}/2}{I_{Dsat}}\right) = \frac{3}{4}\frac{V_{DD}}{I_{Dsat}}$$

$$R_n = R_{eqn}\left(\frac{L_n}{W_n}\right)$$

$$R_p = R_{eqp}\left(\frac{L_p}{W_p}\right)$$

Physical and Material Constants

Name	Symbol	Value	Units
Electron Charge	q	1.6×10^{-19}	C
Boltzmann's Constant	k	1.38×10^{-23}	J °K^{-1}
Room Temperature	T	300	°K (27°C)
Thermal Voltage	$V_{th} = kT/q$	26	mV (at 27°C)
Dielectric Constant of Vaccum	ε_0	8.85×10^{-14}	F cm^{-1}
Dielectric Constant of Silicon	ε_{si}	$11.7\varepsilon_0$	F cm^{-1}
Dielectric Constant of SiO_2	ε_{ox}	$3.97\varepsilon_0$	F cm^{-1}
Carrier Saturation Velocity	v_{sat}	8×10^6	cm s^{-1}
Aluminum Resistivity	ρ_{Al}	2.7	$\mu\Omega$ cm
Copper Resistivity	ρ_{Cu}	1.7	$\mu\Omega$ cm
Tungsten Resistivity	ρ_{W}	5.5	$\mu\Omega$ cm

Wire Resistance, capacitance and Elmore delay

$$C_{wire} \approx \frac{w'\varepsilon_{ox}}{t_{ox}} + \frac{2\pi\varepsilon_{ox}}{\log(t_{ox}/H)}, w' = W - \frac{H}{2}$$
$$R_{wire} = \frac{\rho L}{A} = \frac{\rho L}{HW}$$
$$R_{ik} = \sum R_j, R_j \in [\text{path}(s \to i) \cap \text{path}(s \to k)]$$
$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Typical wire area capacitance per unit wire area (aFμm^{-2})

	Bottom						
Top	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
Al1	30	41	57				
Al2	13	15	17	36			
Al3	8.9	9.4	10	15	41		
Al4	6.5	6.8	7	8.9	15	35	
Al5	5.2	5.4	5.4	6.6	9.1	14	38

Typical wire fringe capacitance per unit wire length, *per side* (aFμm^{-1})

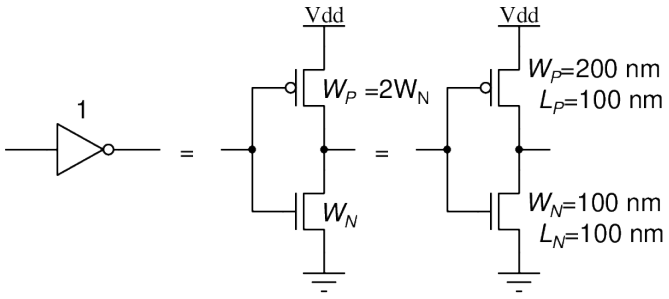
	Bottom						
Top	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	54						
Al1	40	47	54				
Al2	25	27	29	45			
Al3	18	19	20	27	49		
Al4	14	15	15	18	27	45	
Al5	12	12	12	14	19	27	52

Typical inter-wire capacitance per unit wire length (aFμm^{-1}), minimally spaced

Layer	Poly	Al1	Al2	Al3	Al4	Al5
Capacitance	40	95	85	85	85	115

The Standard Inverter

0.13 μm generic technology. Intrinsic delay t_{p0}



Logical Effort (Multi-level Logic Circuits)

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{fi}{bi} \qquad G = \prod_1^N gi \qquad D = t_{p0} \sum_{j=1}^N \left(p_j + \frac{f_i g_i}{\gamma} \right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{\min} = t_{p0} \sum_{j=1}^N \left(p_j + \frac{\sqrt[N]{H}}{\gamma} \right)$$

Intrinsic delay

Gate Type	p
Inverter	1
n-input NAND	n
n-input NOR	n
n-way multiplexer	$2n$
XOR, XNOR	$n2^{n-1}$

Logical effort

g	*Number of inputs*			
Gate Type	1	2	3	n
Inverter	1			
NAND		4/3	5/3	$(n+2)/3$
NOR		5/3	7/3	$(2n+1)/3$
Multiplexer		2	2	2
XOR		4	12	

Engineering Scale and Meter Conversion Factors

G	giga	10^9	c	centi	10^{-2}
M	mega	10^6	m	milli	10^{-3}
k	kilo	10^3	μ	micro	10^{-6}
1 μm = 10^{-4} cm = 10^{-6} m			n	nano	10^{-9}
1 m = 10^2 cm = $10^6 \mu$m			p	pico	10^{-12}
0.1 μm = 100 nm			f	femto	10^{-15}
1 Å = 10^{-8} cm = 10^{-10} m			a	atto	10^{-18}