Version MWCT/3

EGT3
ENGINEERING TRIPOS PART IIB

Tuesday 5 May 2026 9.30 to 11.10

Module 4B28

VERY LARGE SCALE INTEGRATION (VLSI)

CRIB

STATIONERY REQUIREMENTS

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

1 (a) Discuss how process variations in widths and lengths of transistors affects the robustness and performance of a CMOS inverter. [25%]

Solution:

Robustness:

Noise margins of a CMOS inverter is determined by the switching threshold V_M that is dependent on the relative width-to-length ratios of the NMOS and PMOS. A good, stronger NMOS shifts V_M to the left, lowering the low noise margin, while a good, stronger PMOS shifts it to the right, lowering the high noise margin.

As a result, the process variations create inverters with slight different switching thresholds. This effectively reduce the average noise margins to operate the system.

Performance:

The magnitude of drain current is proportional to the width-to-length ratio of a transistor. CMOS inverters drive capacitive loads, and Lower current gives longer propagation delay. Therefore, bad, narrower transistors leads to longer propagation delays that restrict the maximum clock frequency that the system can run on.

(b) A CMOS inverter fabricated in the generic 0.18 μm technology is shown in Fig. 1. The widths of the NMOS and PMOS are 400 nm and 280 nm respectively, and the lengths of the transistors are both 200 nm. There is a capacitive load of 25 pF at its output.

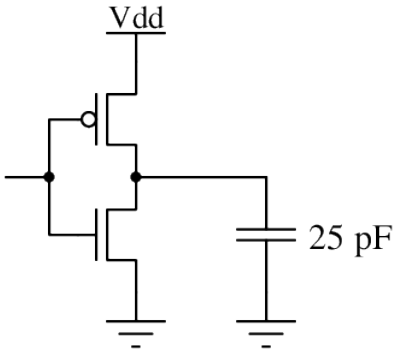


Fig. 1

(i) Estimate the switching threshold V_M of the CMOS inverter. [10%]

(ii) Hence, estimate the maximum instantaneous power of the inverter. [20%]

(iii) Assume a step input from high to low, estimate the propagation delay. State

your assumption. [15%]

Solution:

(i) Assume that both devices have short channels,

$$r = \sqrt{\frac{280}{400} \cdot \frac{200}{200} \cdot \frac{24}{6}} = 1.67$$

$$V_M \approx \frac{1.8 - 0.5 + (1.67)(0.5)}{1 + 1.67} = 0.8\,\text{V}$$

(ii) The instantaneous current drawn from the supply is the maximum at $V_M = 0.8$ V. Drain currents are equal $I_{DN} = |I_{DP}|$.

$$V_{DSATN} = \frac{(0.8 - 0.5)(1.2)}{(0.8 - 0.5) + 1.2} = 0.24 < 0.8$$

NMOS is in velocity saturation mode,

$$I_{DNmax} = (280n \times 100)(8 \times 10^6)(1\mu)\frac{(0.8 - 0.5)^2}{(0.8 - 0.5) + 1.2} = 13.4\mu\text{A}$$

Maximum instantaneous power = $V_{DD} I_{DNmax} = 24.2\ \mu$W

(iii) With a step input from high to low, PMOS is turned OFF. Assume the NMOS is entirely in velocity saturation in the first half of the transient of discharging, then the equivalent resistance model is valid.

$$R_N = (12.5 \times 10^3)(\frac{200n}{280n}) = 8929$$

$$t_p = 0.69 R_N C_L = (0.69)(8929)(25 \times 10^{-12}) = 154\,\text{ns}$$

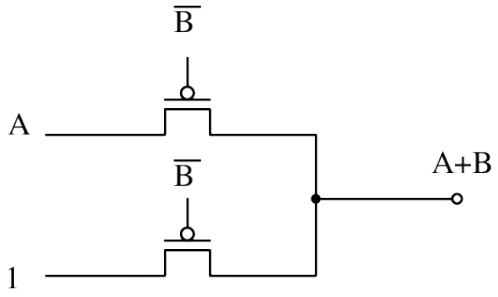
(c) Explain two issues associated with using a single PMOS transistor as a switch. Then, design an OR gate using PMOS pass transistors. Assume both polarities of the input variables A, B, $\overline{A}$ and $\overline{B}$ are available. [30%]

Solution:

Issue 1: PMOS transistors pass a weak 0 due to *threshold drop*, where the output can drop down to only $|V_{Tp}|$.

Issue 2: PMOS pass transistors are more resistive than the NMOS counterpart if fabricated in the same widths, as the mobility of holes is lower than that of the electrons. Width transistors used to compensate the lower mobility of holes requires extra transistor area and thus cost.

Design:



2 Figure 2 shows the typical cross-sectional structure of a *deep-trench* dynamic random access memory (DRAM) cell, fabricated on silicon substrate.

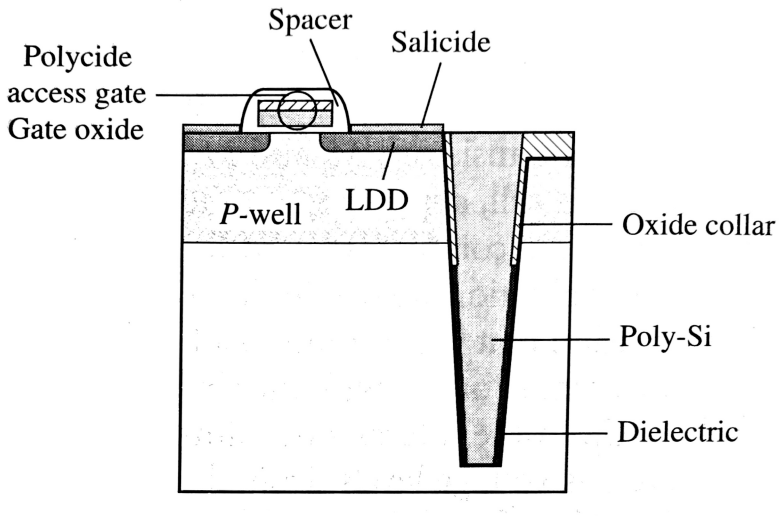


Fig. 2

(a) Describe how the trench could be fabricated using photolithography. Assume that previous layers had been fabricated perfectly. [25%]

Solution:

Assume the access transistor has been fabricated, then the process to create the trench starts with spinning of a layer of photoresist onto the chip. Then the photoresist at the site of the trench is exposed under a mask. The exposed photoresist will dissolve while the unexposed photoresist hardens (assume positive lithography) during development, leaving an opening for the trench.

The chip is then etched heavily and anisotropically to create a deep trench.

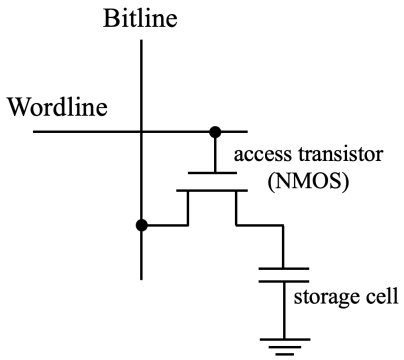
A thin layer of oxide can be formed by oxidating the chip at high temperature for a suitable period, or by using deposition techniques.

After that, polysilicon can be deposited into the deep trench using chemical vapour deposition (CVD) techniques.

Finally, the photoresist is stripped off before the next process.

(b) Draw a labelled circuit schematic for a DRAM cell. [20%]

Solution:



(c) The length and width of the bitline (BL), which is routed on the first aluminum layer (Al1), is 500 μm and 400 nm respectively. The sheet resistance at this layer is 0.1 $\Omega\,\square^{-1}$.

(i) Estimate its lumped resistance and capacitance, assuming that the interconnect is entirely over active transistor area. Ignore the effect of inter-wire capacitance. [20%]

(ii) The DRAM cell storage capacitance C_S is measured as 20 pF. The sensing requirement on the bitline BL is ΔV = 80 mV, which is given by the equation:

$$\Delta V = V_{BL} - V_{BLP} = (V_{cell} - V_{BLP})\frac{C_S}{C_S + C_{BL}}$$

Suggest appropriate operating voltages for precharge, bitline V_{BLP} and cell storage V_{cell}. [15%]

Solution:

(i) Lumped resistance = $\dfrac{500 \times 10^{-6}}{400 \times 10^{-9}} \cdot 0.1 = 125\,\Omega$

Using the tables from the datasheet,

lumped capacitance = $(41 \times 10^{-15})(500)(0.4) + 2 \cdot (47 \times 10^{-15})(500) = 55.2$ pF

(ii) $\Delta V = (V_{cell} - V_{BLP})\dfrac{20}{20 + 55.2} = 0.266(V_{cell} - V_{BLP}) > 80$ mV

$V_{cell} - V_{BLP} > 0.3$

Consider the threshold drop for the access NMOS transistor, a supply V_{DD} of 1.8 V will result at $V_{cell} = 1.8 - 0.5 = 1.3$ V. The bitline precharge voltage is usually half of the supply so $V_{BLP} = 0.9$ V will satisfy the requirement.

(Note: other reasonable suggestion and explanation in the range of $1.2 < V_{DD} < 1.8$ are accpetable)

(cont.

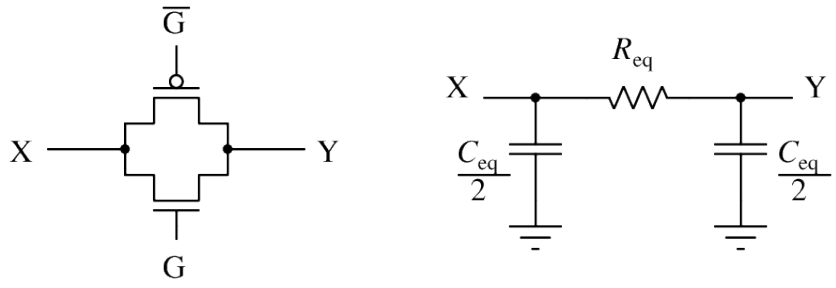
(d) Account for key sources of power dissipations around the DRAM cell. [20%]

Solution:

The subthreshold current in the access transistor and the quantum tunneling effect of electrons give leakage current and static power dissipation.

There is also dynamic power dissipation when the storage cells are charged and discharged during cycles. This includes the periodic refresh required for DRAM.

3 Figure 3(a) and (b) shows a transmission gate and its equivalent π-model respectively.



(a) Transmission gate (b) π -model

Fig. 3

(a) What is the primary source of parasitic capacitance for the transmission gate at points X and Y? Explain how you would estimate the equivalent resistance R_{eq} when it is turned on with $V_{\text{G}} = V_{DD}$. [25%]

Solution:

Diffusion capacitance is the primary source at points X and Y. Source or diode forms capacitors with the body, where the depletion layer acts as a dielectric.

Both NMOS and PMOS are turned ON under $V_{\text{G}} = V_{DD}$. For either of the transistors, the amount of drain current I_{DS} can be estimated at different V_{DS}, and that can be used to calculate the average equivalent resistance by V_{DS}/I_{DS}. The resistance of the transmission gate is the parallel of the two transistors.

(b) Consider the circuit constructed with a number of identical transmission gates in Fig. 4.

 (cont.

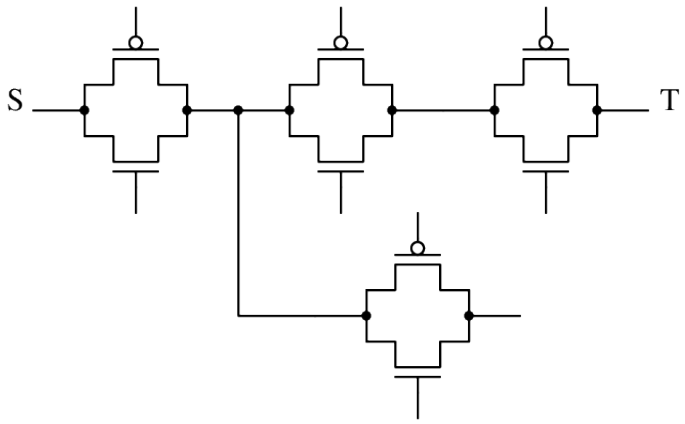
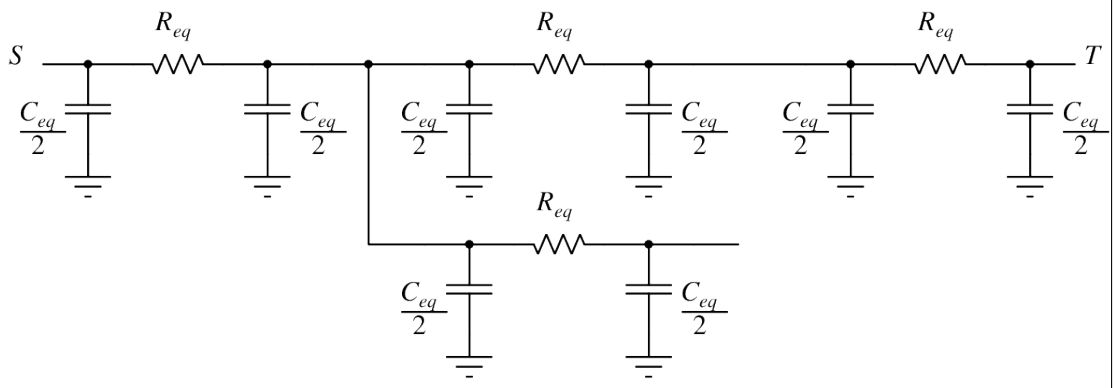


Fig. 4

Now given that R_{eq} = 35 kΩ and C_{eq} = 30 pF, calculate the Elmore delay at T by sketching an equivalent RC tree for the circuit. Assume a step input at S. [30%]

Solution:



Elmore delay at T:

$\tau_T = R_{eq} \cdot \frac{3}{2}C_{eq} + 2R_{eq}C_{eq} + 3R_{eq} \cdot \frac{1}{2}C_{eq} = 5(35 \times 10^3)(30 \times 10^{-12}) = 5.25\ \mu$s.

(c) Transmission gates can be used to build a two-stage positive-edge triggered flip-flop with synchronous reset, as illustrated in Fig. 5.

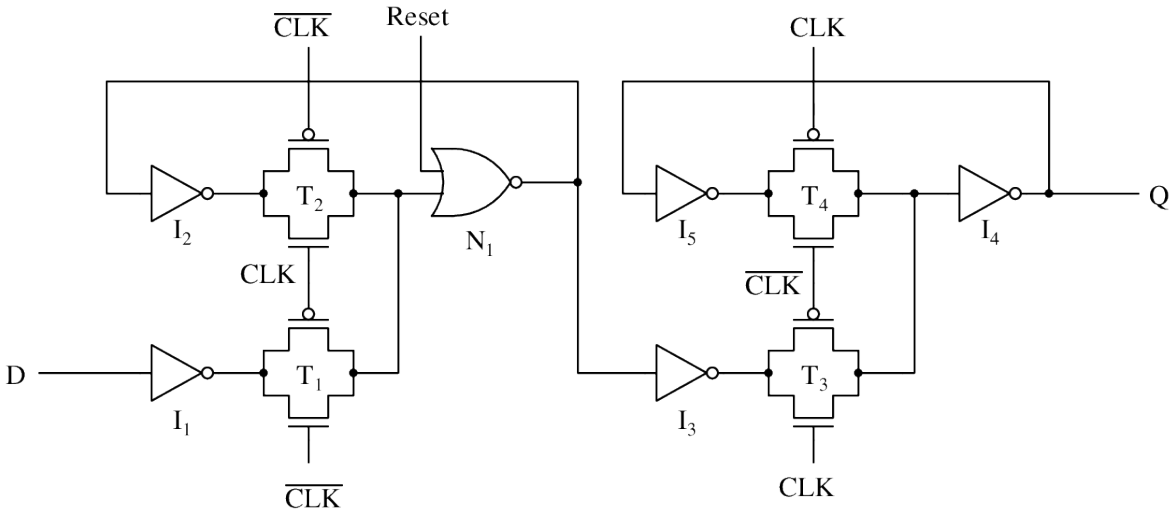


Fig. 5

(i) Estimate the number of transistors required for this circuit. [15%]

(ii) Derive, with explanation, the expression for setup time, hold time and propagation delay of this flip-flop in terms of the propagation delays of the inverters (d_{inv}), NOR gate (d_{nor}) and transmission gates (d_{tg}). [30%]

Solution:

(i) 4 transmission gates = 8 transistors, 5 inverters = 10 transistors and 1 NOR gate = 4 transistors, so 22 transistors in total.

(ii) Before the positive clock edge, T_1 and T_4 are closed. The input D sets up in the circuit by propagating through I_1, T_1, N_1, and I_2/I_3 before the clock edge arrives and closes T_2 and T_3.

Setup time = $2d_{inv} + d_{tg} + d_{nor}$

Since T_1 is open right after the clock edge, there is no requirement to hold D any further, therefore

Hold time = 0

Lastly, D sets up at the output of I_3 before the clock edge. After the edge, it propagates through T_3 and I_4 and arrives at the output Q.

Propagation delay = $d_{tg} + d_{inv}$

4 (a) Design a multi-stage OR gate with 32-bit input. The output of the gate has to drive a load of capacitance 2026 times larger than that of the input of the minimum size standard inverter.

(i) What would be an ideal number of stages N for the designed circuit? Justify the choice using the logical effort method. [20%]

(ii) Based on the choice in (i), sketch the logic path of the designed circuit and work out the sizes of all logic gates [25%]

Solution:

Optimal electrical fanout $f_{opt} \approx 4$, so neglect the logical effort

$$N = \frac{\ln(2026)}{\ln(4)} = 5.49$$

Case 1: $N = 4$

4-input NOR, 4-input NAND, 2-input NOR, inverter

$G = \frac{9}{3} \cdot \frac{6}{3} \cdot \frac{5}{3} \cdot 1 = 10$

$P = 4 + 4 + 2 + 1 = 11$

Propagation delay = $t_{p0}(P + 4\sqrt[4]{FG}) = 58.7t_{p0}$

Case 2: $N = 6$

2-input NOR, 2-input NAND, 2-input NOR, 2-input NAND, 2-input NOR, inverter

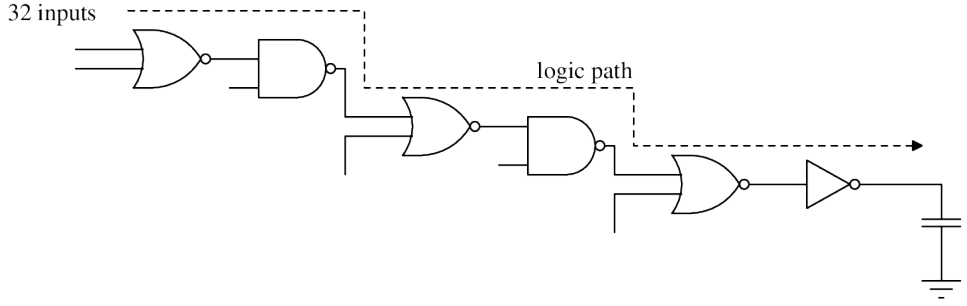
$G = \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot 1 = 8.23$

$P = 2 + 2 + 2 + 2 + 2 + 1 = 11$

Propagation delay = $t_{p0}(P + 6\sqrt[6]{FG}) = 41.3t_{p0}$

Case 2 is better.

Logic path:



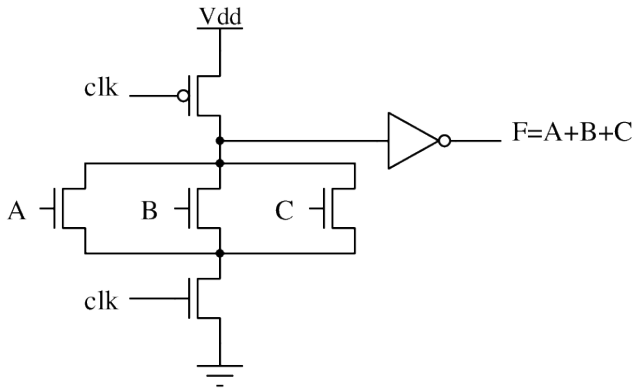
Make the first level NOR gate to has the same input capacitance of the standard inverter, then

$$s_n = \frac{g_1 s_1}{g_n} \prod_{j=1}^{n-1} f_j$$

$g_1 s_1 = 1, s_1 = \frac{3}{5}, h = \sqrt[6]{8.23 \times 2026} \approx 5 = f_1(5/3) \rightarrow f_1 = 3$
Level 2 NAND: $s_2 = \frac{1}{4/3} \cdot 3 = 2.25$
$h = f_2(4/3) = 5 \rightarrow f_2 = 3.75$
Level 3 NOR: $s_3 = \frac{1}{5/3} \cdot 3 \cdot 3.75 = 6.75$
$h = f_3(5/3) = 5 \rightarrow f_3 = 3$
Level 4 NAND: $s_4 = \frac{1}{4/3} \cdot 3 \cdot 3.75 \cdot 3 = 25.3$
$h = f_4(4/3) = 5 \rightarrow f_4 = 3.75$
Level 5 NOR: $s_5 = \frac{1}{5/3} \cdot 3 \cdot 3.75 \cdot 3 \cdot 3.75 = 75.9$
$h = f_5(5/3) = 5 \rightarrow f_5 = 3$
Level 6 inverter: $s_6 = \frac{1}{1} \cdot 3 \cdot 3.75 \cdot 3 \cdot 3.75 \cdot 3 = 379.7$

(b) Design a *domino* OR gate $F = A + B + C$. Assume only the positive phase of the inputs A, B and C are available. Discuss why the domino gate is considerably faster than its static CMOS counterpart. [30%]

Solution:



Input capacitance is reduced because the removal of the pull-up network, consisting of wider PMOS. Propagation delay is proportional to the input capacitance. Furthermore, domino logic has no propagation delay only when the output is logic 1.

(c) Explain the impact of significant skew in the precharge/evaluation clock signal to the reliability of a system built by domino gates. [25%]

Solution:

The period of the percharge/evaluation clock has to be long enough for the logic to propagate through the domino gates. If there is significant skew, the period is effectively reduced, so it is possible that later domino gates could not complete its evaluation and give incorrect results.

END OF PAPER

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