UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIB

Friday 23 April 2004 9 to 10.30

Module 4B18

ADVANCED ELECTRONIC DEVICES

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

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1 (a) Describe, with diagrams and typical layer parameters, the semiconductor multilayer sequence required for a pseudomorphic high electron mobility transistor. [30%]

(b) Describe, with diagrams, and typical sample dimensions the processing steps required to make a pseudomorphic high electron mobility transistor, suitable for operation at 100GHz. [30%]

(c) Outline, with explanations, the performance enhancements achieved as one goes from

(i) a silicon metal-oxide-semiconductor field effect transistor, to
(ii) a gallium arsenide metal-semiconductor field effect transistor, to
(iii) a high electron mobility transistor and
(iv) a pseudomorphic high electron mobility transistor. [40%]

2 (a) Compare and contrast the performances, citing typical figures of merit, that can be achieved with

(i) field-effect transistors and
(ii) bipolar transistors for applications at high frequencies. [30%]

(b) Describe the analytical techniques that would be used in association with a production line to confirm the layer structure and the doping profile of a heterojunction bipolar transistor. What additional techniques are available at the laboratory development phase of the device technology? [30%]

(c) Why is it that heterojunction bipolar transistors have almost totally replaced homojunction bipolar transistors in practical applications? [40%]

3 (a) Describe, with diagrams and appropriate equations, the process of tunnelling through

(i) one thin semiconductor barrier layer, and
(ii) resonant tunnelling through two semiconductor barrier layers. [30%]

(b) Describe two potential applications of tunnelling in electronic devices, and the typical performance figures that are demonstrated in prototype devices. [30%]

(c) Outline the problems associated with the manufacture of tunnel devices and the challenges that have to be met to achieve low-cost manufacture of tunnel devices. [40%]

4 (a) What is meant by the negative differential resistance? Why is it important for device operation? Give three ways of generating negative differential resistance in semiconductor multilayers? [40%]

(b) Describe, with annotated diagrams and typical performance figures, the basic operation of a Gunn diode in gallium arsenide, and the improvements to its performance if a hot-electron injector is incorporated into its cathode. [60%]

5 (a) Describe with reference to the Johnson criteria why gallium nitride is being researched intensively for electronic and optical devices. [50%]

(b) What are the specific challenges associated with multilayers of silicon and silicon-germanium alloys in terms of the applications in mainstream electronic devices, and what is the present status of this materials system in real applications? [50%]

END OF PAPER